Claim Listing

Please cancel claims 9-13, 17-20, and 23-25.

1. (Currently Amended) A processing system ~~for providing a distributed directory based coherence protocol incorporating prefetching buffers~~, comprising:

a memory [[hierarchy level having]] comprising a coherence directory and associated coherence directory data, wherein the coherence directory comprises a plurality of memory blocks each having different corresponding coherence directory data;

a plurality of prefetch address registers;

~~a plurality of memory blocks each associated with different directory data;~~

a plurality of buffers interconnected to said memory;

a plurality of processing elements, each said processing element interconnected to a different [buffers] one of said plurality of buffers;

wherein each of the processing elements comprises requesting means for requesting a selected one of said memory blocks from said memory;

wherein the memory comprises means [[associated with said memory,]] responsive to said requesting means [[for requesting for delivery]], ~~in response to said requesting,~~ for [[delivery of a corresponding]] providing the selected memory block ~~of said memory blocks, a corresponding set of said~~ , the coherence directory data [[from said memory,]] corresponding to the selected memory block, and contents of at least one of the prefetch address registers to [[an associated element]] a requesting one of said

processing elements ~~, further incorporating the value of prefetch address registers in said response~~; and

wherein each of the processing elements comprises means [[for said processing elements]] for ~~detecting said delivery of said~~ receiving the selected memory block, the coherence directory data corresponding to the selected memory block, and the contents of the at least one of the prefetch address registers, and is configured to determine if [[said]] the [[delivered]] selected memory block [[of said processing element]] is available for a particular access mode ~~, and if not, performing coherence actions corresponding to said coherence directory data~~.

2. (Currently Amended) The system of Claim 1, wherein the processing elements are connected with said buffers [[connected to the memory]] via point to point links.

3. (Currently Amended) The system of Claim 1, wherein the [[process of incorporating the value]] contents of the at least one prefetch address register is ~~performed by including the value of at least one prefetch address register from said memory hierarchy level as~~ a field in [[said]] a response.

4. (Currently Amended) The system of Claim 1, wherein the [[process of incorporating the value]] contents of the at least one prefetch address register [[comprises]] is included in a transmitted directory information modifier ~~, indicating for the coherence directory information, the combined coherence information stored in the memory hierarchy level in the coherence directory entries and the prefetch address registers~~.

5. (Currently Amended) The system of Claim 1, wherein ~~the response generated includes a plurality of memory blocks and their associated directory coherence entries~~ the memory comprises means responsive to said requesting means for providing a plurality of memory blocks including the selected memory block, the coherence directory data corresponding to the plurality of memory blocks, and contents of at least one of the prefetch address registers to a requesting one of said processing elements.

6. (Currently Amended) The system of Claim 5, wherein the plurality of [[the]] memory blocks and the [[associated]] coherence directory data corresponding to the plurality of memory blocks [[transmitted in the response]] are stored in a prefetch buffer, and the contents of the at least one of the prefetch address register comprises an identifying address of said plurality of memory blocks ~~is stored in at least one of the prefetch address register in said memory hierarchy level~~.

7. (Currently Amended) The system of Claim 6, wherein each of the processing elements is configured to use a prefetched plurality of memory blocks stored in a prefetch buffer [[are employed]] to provide memory data if said [[stored]] coherence directory data corresponding to the selected memory block indicates ~~compatible access modes for one of shared and both shared and exclusive memory access modes~~ the selected memory block is available for either: (i) a shared access mode, or (ii) both the shared access mode and an exclusive access mode.

8. (Currently Amended) The system of claim 7, wherein [[an]] the identifying address stored in said at least one prefetch register indicates that said ~~memory block within said indicated prefetch block~~ plurality of memory blocks [[may be used]] is available for ~~one of shared and both shared and~~

~~exclusive access~~ either: (i) the shared access mode, or (ii) for both the shared access mode and the exclusive access mode.

9. (Canceled).

10. (Canceled).

11. (Canceled).

12. (Canceled).

13. (Canceled).

14. (Currently Amended) A method for ~~implementing a distributed directory based coherence protocol supporting the presence of prefetch buffers~~ providing memory data to a requestor of the memory data, the method comprising:

requesting a memory block from a memory hierarchy level having a coherence directory, associated coherence directory data, and a plurality of prefetch address registers[[,]];

generating a response including the memory data and corresponding coherence [[information]] directory data[[,]];

updating the directory [[information]] coherence data corresponding to the memory data and indicating the address of a prefetched block in a prefetch address register[[,]];

receiving [[a]] the response including the memory data and the corresponding coherence [[information]] directory data from said memory hierarchy level[[,]];

~~a testing step to indicate~~ determining whether the received coherence [[information]] directory data is compatible with a required access mode[[,]];

[[a step of]] performing at least one coherence action[[s]] if ~~said test indicates one of incompatibility, and possible incompatibility~~ the received coherence directory data is incompatible with the required access mode[[,]]; and

[[a step of]] providing the memory data [[which has been obtained]] to [[a]] the requestor of the memory data.

15. (Currently Amended) The method of Claim 14, wherein the providing ~~said coherence information provides separate~~ comprises providing the memory data and the coherence directory [[information]] data ~~and prefetch address information~~ to a requestor of the memory data.

16. (Currently Amended) The method of Claim 15, wherein ~~providing said coherence information provides merged coherence data, said~~ the provided coherence directory data comprises merged coherence data [[having been obtained]] generated by combining [[the]] information contained in at least one coherence directory entry and at least one prefetch address register.

17. (Canceled).

18. (Canceled).

19. (Canceled).

20. (Canceled).

21. (Currently Amended) The method of Claim 14, wherein [[requests and responses]] the requesting of the memory block and the generating and receiving of the response are [[performed]] carried out by sending and receiving data over [[logical]] point to point links.

22. (Currently Amended) The method of Claim 14, wherein at least one of the prefetch address registers stores [[at least]] a prefetch address and a prefetch data length.

23. (Canceled).

24. (Canceled).

25. (Canceled).

Please add the following new claims:

26. (New) A method for providing needed data to a processing element, the method comprising:

receiving the needed data and coherence directory data corresponding to the needed data;

using the received coherence directory information to determining a condition of the needed data;

determining if the condition of the needed data is compatible with a required access mode;

in the event the condition of the needed data is compatible with the required access mode, providing the needed data to the processing element.

27. (New) The method as recited in claim 26, further comprising:

in the event the condition of the needed data is not compatible with the required access mode, performing at least one coherence action.